DMA CONTROLLER MODES OF OPERATION

BLOCK TRANSFERS (BURST MODE) => DMA takes control of the memory bus from CPU, transfers ALL data, & then returns bus to CPU.

CYCLE STEALING => DMA controller transfers a single byte whenever it can acquire the bus from the CPU, then releases the bus to the CPU. Waits for the next opportunity (ie. Next time it releases bus)

TECHNIQUES FOR DMA BUFFEREING & CPU PROCESSING

SIGNLE BUFFERED DMA – DMA reads data blocks & fills buffer. Once the buffer is full, the uP then reads the data & computes on the blocks of data as programmed. The DMA reads the next data block etc.

However, the rate at which the blocks are processed depends on the time required to fill the buffer by the DMA.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| DMA WRITING TO | BUFFER |  | BUFFER |  | ... |  |
| CPU READING FROM |  | BUFFER |  | BUFFER | ... |  |

DOUBLE BUFFERED DMA

2 dedicated buffers for DMA accesses. When one DMA is filling one of the buffers, the CPU is reading and processing the other buffers data. Once both the DMA and CPU are finished with their bufferes, they swap buffers and repeat the process.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| DMA WRITING TO | BUFFER1 | BUFFER2 | BUFFER1 |  | ... |  |
| CPU READING FROM |  | BUFFER1 | BUFFER2 | BUFFER1 | ... |  |